UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/868,322	06/18/2001	Yojiro Matsueda	109503	9116

25944 7590 05/16/2005

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
NGUYEN, JENNIFER T	
ART UNIT	**PAPER NUMBER**
2674	

DATE MAILED: 05/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/868,322	MATSUEDA, YOJIRO	
	Examiner	Art Unit	
	Jennifer T Nguyen	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 June 2001*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *27-37 and 43-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *27-37,43,44 and 46-53* is/are rejected.

7)☒ Claim(s) *45* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is responsive to amendment filed on 12/20/2004.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 27-31, 33-37 and 46-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda et al. (U.S. Patent No. 5,815,136) in view of Kumagai et al. (U.S. Patent No. 5,440,718) and further in view of Quanrud (U.S. Patent No. 6,339,417).

Regarding claims 27 and 47, referring to Figs. 47A and 47B, Ikeda teaches a display device, comprising: a display section (2451) having a plurality of scanning lines and a plurality of data lines formed in a grating form corresponding to dots as minimum units of display and active elements provided corresponding to intersections; a scanning line driver (2449) that selects and drives the scanning lines; a memory (2425) having a plurality of memory cells that are capable of storing an image signal for performing display control of dots in at least one row of the display section (2451); a column decoder (2443) that selects the memory cells for storing an input-image signal; a column selection switch section (2445) to switch on the basis of a selection by the column decoder (2443) and the image signal and storing the image signal to said memory cells selected by said column decoder (2443); and a data line driver (2405) that drives said data lines on the basis of the image signal stored in the memory (2425) (from col. 31, line 40 to col. 33, line 67 and col. 34, lines 28-65).

Ikeda differs from claims 27 and 47 in that he does not specifically teach the plurality of memory cells being arranged in a matrix having a plurality of rows and a plurality of columns and the memory being disposed between the display section and the column selection switch section, and the display section, the memory, and the column selection switch section being formed on one substrate. However, referring to Fig. 1, Kumagai teaches a plurality of memory cells (MC) being arranged in a matrix (i.e., memory cell array 10) having a plurality of rows and a plurality of columns and the memory (10) being disposed between the display section (not shown) and the column selection switch section (12), wherein the memory (10), and the column selection switch section (12) being formed on one substrate (52) (from col. 3, line 64 to col. 4, line 18 and col. 7, lines 18-26) and Quanrud teaches display section, selection switch section and the memory being formed on one substrate (col. 5, lines 12-20). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to in corporate the memory cells being arranged in a matrix having a plurality of rows and a plurality of columns and the memory being disposed between the display section and the column selection switch section as taught by Kumagai and the display section, the memory, and the column selection switch section being formed on one substrate as taught by Quanrud in the system of Ikeda in order to provide a driving circuit can be small-sized as a whole, according power consumption in the driving circuit can be reduced.

Regarding claim 29, Ikeda further teaches a plurality of word lines among which a word line is selected when a memory cell of the plurality of memory cells receives the image signal, the plurality of word lines extending along a row direction that intersects a column direction along which the plurality of data lines extend (Fig. 1A and 15).

Regarding claims 28 and 49-52, Ikeda further teaches the memory cell section (2425) storing image signals for one screen (2451) (Fig. 1, 15, 17A, and 17B, from col. 31, line 40 to col. 33, line 67).

Regarding claims 30-31, Ikeda further teaches on the basis of an address signal representative of a display position and a storage position, said scanning line driver selects the scanning lines and the word line driver selects said word lines (Fig. 1A, col. 9, lines 19-67).

Regarding claims 33, 34, 36, and 42 the combination of Ikeda, Kumagai, and Quanrud teaches the plurality of the memory cell section being configured by a dynamic memory (col. from col. 3, line 64 to col. 4, line 18 of Kumagai).

Regarding claim 35, Ikeda teaches only when a change of display in one dot of the plurality of dots is carried out, a memory cell of the plurality of memory cells that corresponds to the one dot receiving the image signal (Figs. 17A and 17B) (col. 14, lines 13-49).

Regarding claims 37 and 48, referring to Figs. 47A and 47B, Ikeda teaches a display device, comprising: a display section (2451) having a plurality of scanning lines and a plurality of data lines formed in a grating form corresponding to dots as minimum units of display and active elements provided corresponding to intersections; a scanning line driver (2449) that selects and drives the scanning lines; a memory (2425) having a plurality of memory cells that are capable of storing an image signal for performing display control of dots in at least one row of the display section (2451); a column decoder (2443) that selects the memory cells for storing an input-image signal; a column selection switch section (2445) to switch on the basis of a selection by the column decoder (2443) and the image signal and storing the image signal to said memory cells selected by said column decoder (2443); and a data line driver (2405) that drives

said data lines on the basis of the image signal stored in the memory (2425) (from col. 31, line 40 to col. 33, line 67 and col. 34, lines 28-65).

Ikeda differs from claims 37 and 48 in that he does not specifically teach the plurality of memory cells being arranged in a memory cell section having a plurality of rows and a plurality of columns, the length of the matrix in a row direction extend being shorter than a length of the display section in the row direction, the memory cell section, and the column selection switch section being formed on one substrate. However, referring to Fig. 1, Kumagai teaches a plurality of memory cells (MC) being arranged in a matrix (i.e., memory cell array 10) having a plurality of rows and a plurality of columns and the memory (10) being disposed between the display section (not shown) and the column selection switch section (12) (from col. 3, line 64 to col. 4, line 18 and col. 7, lines 18-26) and Quanrud teaches display section, selection switch section and the memory being formed on one substrate (col. 5, lines 12-20) and it is the matter of design choice to obtain the length of the matrix in a row direction extend being shorter than a length of the display section in the row direction. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to in corporate the plurality of memory cells, the length of the matrix in a row direction extend being shorter than a length of the display section in the row direction, and the memory being disposed between the display section and a selection switch section, the display section, the memory cell section, and the column selection switch section being formed on one substrate as taught by Kumagai and Quanrud in the system of Ikeda in order to provide a driving circuit can be small-sized as a whole, according power consumption in the driving circuit can be reduced.

Regarding claim 46, Ikeda teaches a column decoder (112) that selects a memory cell of the plurality of memory cells by cooperation with the word line (Figs. 1A and 15) (from col. 31, line 40 to col. 33, line 67 and col. 34, lines 28-65).

Regarding claim 53, Ikeda teaches a gray scale level in the display section being obtained by an area gray scale method (Fig. 21, col. 16, line 52 to col. 17, line 35).

4. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda et al. (U.S. Patent No. 5,815,136), Kumagai et al. (U.S. Patent No. 5,440,718) in view of Quanrud (U.S. Patent No. 6,339,417) and further in view of Koyama et al. (U.S. Patent No. 6,111,557).

Regarding claim 32, the combination of Ikeda, Kumagai, and Quanrud differs from claim 32 in that it does not specifically teach a DAC section having a plurality of DACs, each of the plurality of DACs receiving digital data based on the image signal, each of the plurality of DACs converting the digital data into analog data. However, referring to Fig. 1, Koyama teaches a DAC section having a plurality of DACs, each of the plurality of DACs receiving digital data based on the image signal, each of the plurality of DACs converting the digital data into analog data (col. 5, line 48 to col. 6, line2). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to in corporate the DAC section as taught by Koyama in the system of the combination of Ikeda, Kumagai, and Quanrud in order to provide a correspond an analog signal to display image successfully.

5. Claim 45 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. Applicants' arguments filed 12/20/04, have been fully considered but they are not persuasive because as follows:

In response to Applicants' argument filed "Applicant respectfully disagrees with the Office Actions's assertion that Quanrud provides the deficiencies of Ikeda. Instead, the memory cell disclosed in Quanrud is disposed corresponding to each pixel and acts as a pixel circuit to drive each pixel". However, the Office action rejected claim 27 by the combination of Ikeda, Kumagai and Quanrud. Referring to Fig. 1, Kumagai teaches a plurality of memory cells (MC) being arranged in a matrix (i.e., memory cell array 10) having a plurality of rows and a plurality of columns and the memory (10) being disposed between the display section (not shown) and the column selection switch section (12), wherein the memory (10), and the column selection switch section (12) being formed on one substrate (52) (from col. 3, line 64 to col. 4, line 18 and col. 7, lines 18-26) and Quanrud teaches display section, selection switch section and the memory being formed on one substrate (col. 5, lines 12-20). Moreover, referring to Fig. 15, Ikeda also teaches a plurality of memory cells being arranged in a matrix having a plurality of rows and a plurality of columns (col. 13, line 62 to col. 14, line 6). Applicant also argued that "none of the applied references disclose or suggest a length of the memory cell section in a row direction that intersects the column direction along with the plurality of data lines extend, being shorter than a length of the display section in a row direction". However, the length of memory cell section in row direction being shorter than the length of the display section in a row direction is obtained by smaller in size of each cell. In re Rose, 105 USPQ 237 (CCPA 1955), change in size is matter of design choice. We do not fell that this limitation is patentably significant since it is most

relates to the size of the article under consideration which is not ordinarily a matter of invention. In re Yount, 36 C.C.P.A. (Patent) 755, 171 F2d 317, 80 USPQ 141. Applicant also argued "There is no motivation or suggestion to combine the device of Ikeda with the memory device of Kumagai. Examiner disagrees because Ikeda system teaches memory cell section. However, he does not specifically teaches the details of the memory cell section. Kumagai teaches the detail of the memory cell section (i.e., memory cells being arranged in a matrix having a plurality of rows and a plurality of columns). This is combination and subcombination rejection and it is proper to combine the memory cell section of Ikeda and the memory cell section of Kumagai. Therefore, the ground of the rejection is maintained.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer T Nguyen whose telephone number is 571-272-7696. The examiner can normally be reached on Mon-Fri: 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick N. Edouard can be reached on 571-272-7603. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JNguyen
5/4/05

REGINA LIANG
PRIMARY EXAMINER